

ABSTRACT OF THE DISCLOSURE

A decode unit is coupled to receive instruction bytes and to dispatch instructions
5 to an execution subsystem. The decode unit comprises circuitry divided into a pipeline
including a plurality of pipeline stages, wherein the circuitry is configured to concurrently
initiate decode of a plurality of instructions and to dispatch at least an initial instruction of
the plurality of instructions from a first pipeline stage of the plurality of pipeline stages.
Furthermore, the circuitry is configured to dispatch at least one remaining instruction of
10 the plurality of instructions from a second pipeline stage of the plurality of pipeline
stages. The second pipeline stage is subsequent to the first pipeline stage in the pipeline.